Carrier Freeze-out and Relaxation Effects in CMOS N-channel MOSFETS at Cryogenic Temperatures Under Dynamic Operating Conditions

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The operation of semiconductor circuits at low temperatures is motivated by improved device and circuit performance, potential application of superconducting films, and the need for low noise amplifier circuits to operate with low noise sensors. However N-channel CMOS transistors contained in a P-well and operated at very low temperatures (¡30 K) exhibit a kink and associated hysteresis, which makes them unsuitable for linear amplification [1-4]. The kink is attributed to impact-ionization near the drain, in conjunction with a floating substrate. Impact ionization near the drain generates majority carriers that are collected at the source and thus provide a bias to the well. The well bias decreases the threshold voltage of the transistor and the current increases. At a particular drain voltage, which is called the kink voltage, the current saturates at a higher value. At room temperature, floating the well results in the generation of substrate current, a slight increase in leakage currents, and degradation of latch-up immunity. These effects are all minimized at low temperatures. However, hot carrier degradation is aggravated at low temperatures due to the higher electric fields and increased electron mean free path. Hot electron degradation at low temperature is seen in an increased threshold voltage shift, increased transconductance degradation and decreased device lifetimes [5].

In this paper we present the results of Id Vd and hot electron degradation studies conducted on N-channel MOSFETS contained in a P-well at cryogenic operating temperatures. It is found that at cryogenic temperatures (13 25 K), floating the well contact eliminates the kink after the first Id Vd characteristic, and the drain current is consistent with the current at high drain voltages measured with the well contact grounded. It appears that the well bias generated at the kink does not relax when the well is floating which reduces the field at the drain. Hot electron degradation of n-channel MOSFETs in a P-well at 25 K for two stressing conditions was studied. For one stress condition, dynamic stress was done with the well grounded and for the second stressing condition the well was floating during stress. Degradation was seen in the linear region and in inverse mode, which was not observed in saturation in the forward mode. This indicates that negative charge at the interface near the drain has resulted. Comparison of the linear region transconductance degradation for the two devices shows increased degradation of the device stressed with the well grounded. Floating the well allows the well bias, once induced, to remain and decreases the field at the drain which reduces hot electron degradation. As an additional consequence of the reduced drain field, negative charge is concentrated closer to the drain and a decrease in the kink voltage is seen after stress.

References

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